

## 6-line IPAD™, EMI filter and ESD protection for SD card

### Features

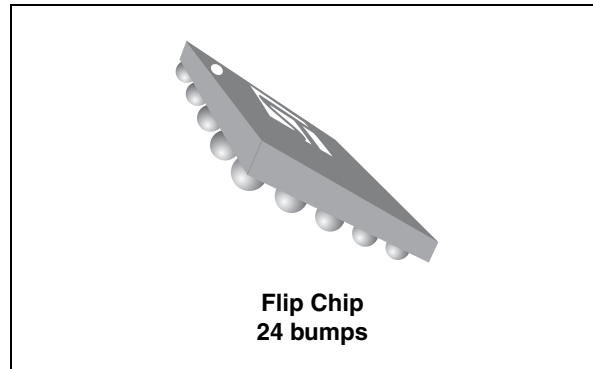
- ESD protection (IEC standard)
- EMI Filtering
- Level translator
- Signal conditioning
- Integrated power supply with:
  - Thermal shutdown (TSD)
  - Under voltage lockout (UVLO)
  - Short-circuit current limitation ( $I_{SC}$ )
  - Power on/off feature with Enable pin.

### Benefits

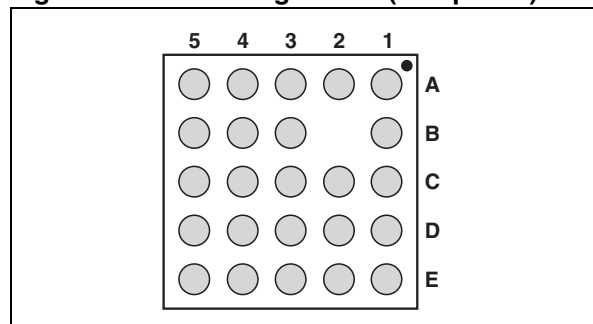
- EMI Low-pass-filter and ESD protection (up to 15 kV on external pins)
- Integrated pull up resistors to prevent bus floating
- 50 MHz clock frequency compatible with  $C_{line} < 40$  pF
- Lead-free package in 400  $\mu$ m pitch
- Low power consumption
- Very low PCB space consumption
- High reliability offered by monolithic integration
- Reduction of parasitic elements thanks to CSP integration

### Complies with the following standards

- IEC 61000-4-2, Level 4 (external pins)
  - 15 kV (air discharge)
  - 8 kV (contact discharge)
- HBM IEC 61340-3-1 (all pins)
  - 2 kV (air discharge)
  - 2 kV (contact discharge)



**Figure 1. Pin configuration (bump side)**



### Applications

- Removable memory cards in mobile phones, communication systems, and portable applications
- Memory cards compliant with: SD (standard and high speed), MiniSD,  $\mu$ SD and MMC/Trans-flash standards

### Description

The EMIF06-SD02F3 is a highly integrated device, based on IPAD technology, combining 5 functions. The Flip-Chip packaging means the package size is equal to the die size.

TM: IPAD is a trademark of STMicroelectronics.

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# 1 Functional description

## A SIDE (Host-CPU) pin list:

$V_{ccA}$ , Enable, Dat123.dir, CMD.dir, CMD.h, CLK.h, CLK-f, Dat0.dir, Dat0.h, Dat1.h, Dat2.h, Dat3.h,  $V_{bat}$

## B SIDE (SD-Card) pin list:

WP, CD,  $V_{ccB}$ , CMD-B, CLK-B, Dat0-B, Dat1-B, Dat2-B, Dat3-B

**Table 1. Pin definition**

Pin Name	Bump	Type	Side	Description
$V_{ccA}$	B3	Power input	A	Power supply (1.8v)
$V_{ccB}$	B4	Power output	B	Power supply (internally generated, 2.9 V)
$V_{bat}$	A4	Power input	A	Battery power supply
GND	C4	Ground	-	Ground
GND	C3	Ground	-	Ground
Enable	C2	Input	A	Internal power supply enable
CMD.dir	A2	Input	A	Command direction
CMD.h	D2	IO	A	A side command
CLK.h	C1	Input	A	Clock input
CLK-f	E2	Output	A	Clock feedback
Dat0.dir	A3	Input	A	Data direction
Dat0.h	D1	IO	A	Data host
Dat123.dir	E3	Input	A	Data direction
Dat1.h	E1	IO	A	Data host
Dat2.h	A1	IO	A	Data host
Dat3.h	B1	IO	A	Data host
WP	E4	Input to CPU	A	Write protect
CD	D3	Input to CPU	A	Card detect
CMD-B	D4	IO	B	Command direction
CLK-B	C5	Output	B	Clock output
Dat0-B	D5	IO	B	Data SD
Dat1-B	E5	IO	B	Data SD
Dat2-B	A5	IO	B	Data SD
Dat3-B	B5	IO	B	Data SD

Note: In Table 5, 6, 7, and 10, collective names are used for groups of pins. The names used are:

\*.dir = CMD.dir, Dat0.dir, Dat123.dir

\*.h = CMD.h, CLK.h, Dat0.h, Dat1.h, Dat2.h, Dat3.h

\*-B = CMD-B, CLK-B, Dat0-B, Dat1-B, Dat2-B, Dat3-B

$V_{iA}$  = All A side input pins

$V_{iB}$  = All B side input pins.

Table 2. Function table

Command signals				A side signals direction					B side signal direction			
Enable	CMD.dir	Dat0.dir	Dat123.dir	CMD.h	CLK.h	CLK-f	Dat0.h	Dat1.h Dat2.h Dat3.h	CMD-B	CLK-B	Dat0-B	Dat1-B Dat2-B Dat3-B
H	H	X	X	IN	IN	OUT	X	X	OUT	OUT	X	X
H	L	X	X	OUT	IN	OUT	X	X	IN	OUT	X	X
H	X	H	X	X	IN	OUT	IN	X	X	OUT	OUT	X
H	X	L	X	X	IN	OUT	OUT	X	X	OUT	IN	X
H	X	X	H	X	IN	OUT	X	IN	X	OUT	X	OUT
H	X	X	L	X	IN	OUT	X	OUT	X	OUT	X	IN
L	X	X	X	X	X	Z	X	X	L*	Z	L*	L*

- Note: 1 When A side signals direction is INPUT, SD-CARD is WRITTEN by CPU-Host (i.e B side signals direction is OUTPUT)  
 When A side signals direction is OUTPUT, SD-CARD is READ by CPU-Host (i.e B side signals direction is INPUT)
- 2 For B side signals when Enable = L:  
 \* Defined by internal pull-down (cf Block Diagram for pins CMD.B and data bus Dat[0...3].B)

Figure 2. Configuration

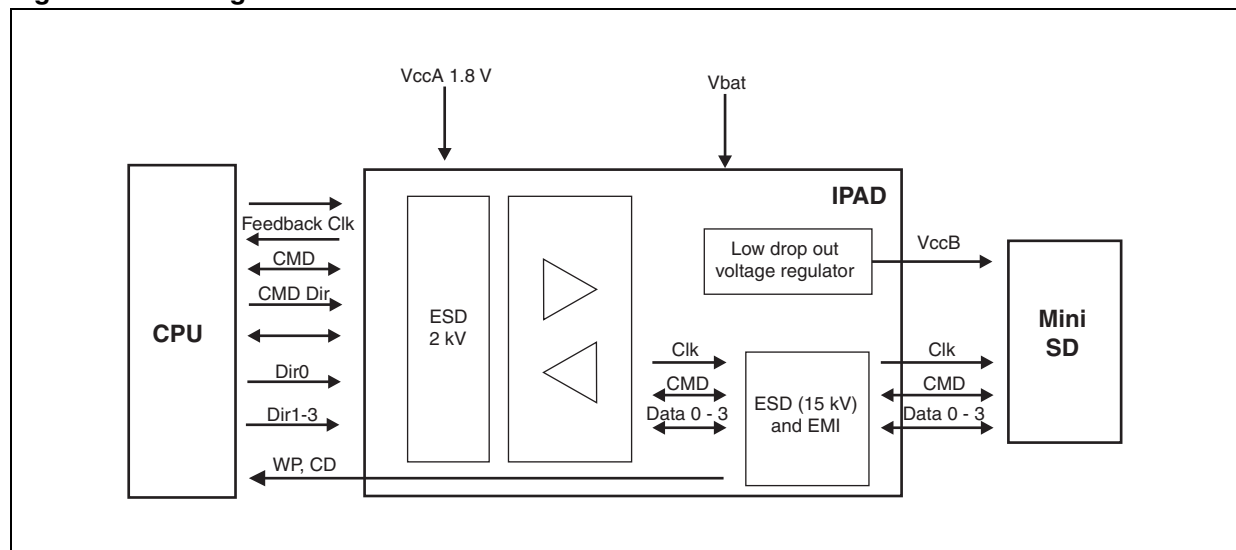
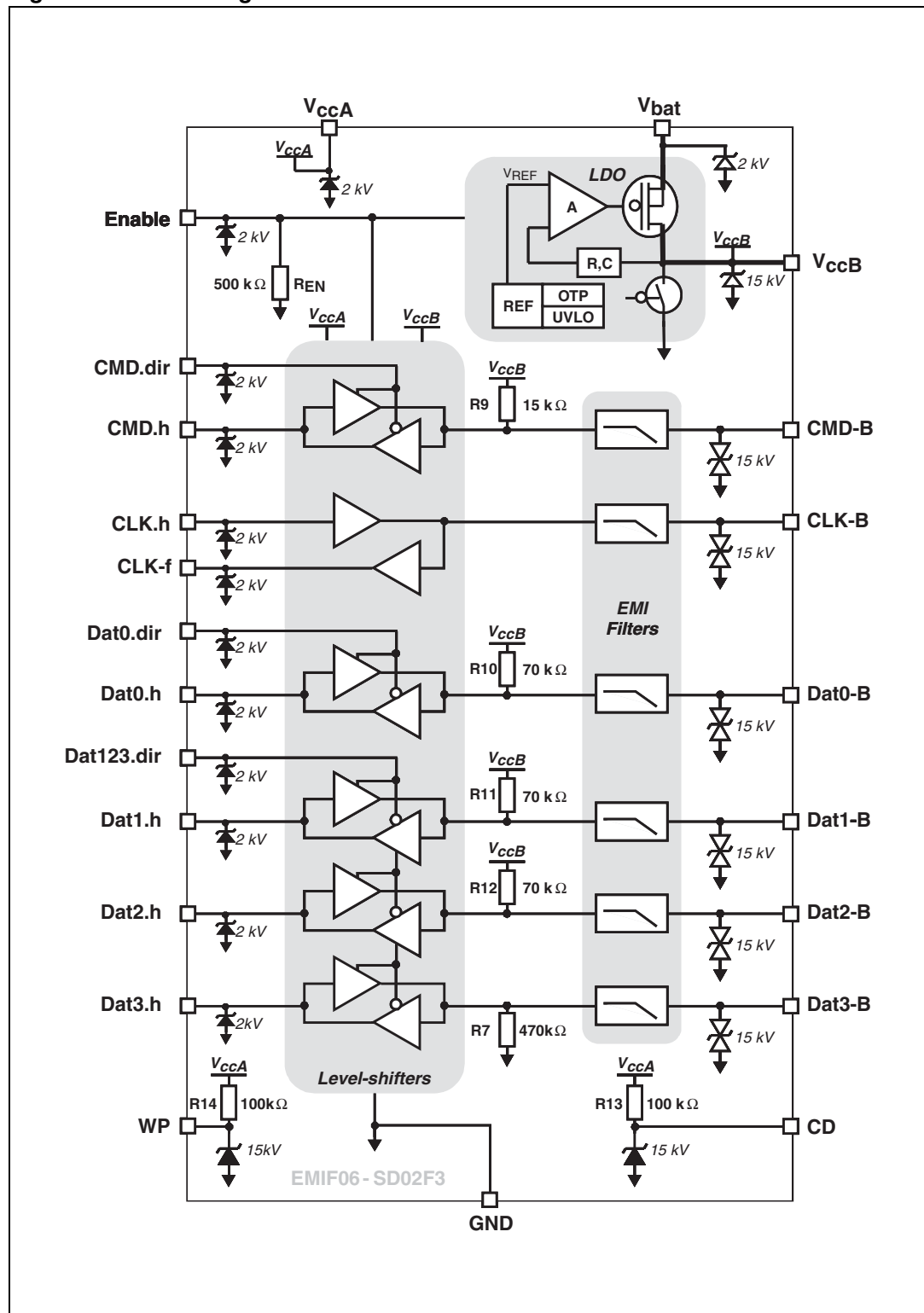


Figure 3. Block diagram



## 2 Characteristics

**Table 3. Absolute maximum ratings**

Symbol	Parameter		Value	Unit
ESD	<b>A SIDE (Host-CPU)</b> <b>All pins: HBM IEC61340-3-1</b> $V_{CCA}$ , Enable, Dat123.dir, CMD.dir, CMD.h, CLK.h, CLK -f, Dat0.dir, Dat0.h, Dat1.h, Dat2.h, Dat3.h, $V_{bat}$	Air discharge Contact discharge	2 2	kV
	<b>B SIDE (SD-Card)</b> <b>External pins : IEC 61000-4-2, level 4</b> $V_{CCB}$ , CMD-B, CLK-B, Dat0-B, Dat1-B, Dat2-B, Dat3-B, WP, CD	Air discharge Contact discharge	15 8	
$T_{jmax}$	Maximum junction temperature		150	°C
$R_{th(j-a)}^{(1)}$	Thermal resistance from junction to ambient Board: epoxy FR4, copper thickness = 40 $\mu m$ , 4 layers		64	°C/W
$P_{dmax}$	Maximum power dissipation: $P_{dmax} = (T_{jmax} - T_{aopmax}) / R_{th(j-a)}$		1	W
$T_{stg}$	Storage temperature range		-55 to +150	°C
Voltage	$V_{bat}$ , $V_{CCB}$ , Enable		-0.3 to 5.5	V
	CMD-B, CLK-B, Dat0-B, Dat1-B, Dat2-B, Dat3-B		-0.3 to $V_{CCB} + 0.3$	
	$V_{CCA}$		-0.3 to 3.3	
	Dat123.dir, CMD.dir, CMD.h, CLK.h, CLK -f, Dat0.dir, Dat0.h, Dat1.h, Dat2.h, Dat3.h, WP, CD		-0.3 to $V_{CCA} + 0.3$	

1.  $V_{CCB}$  is an internally generated power supply, no external voltage should be applied on this pin other than a current clamp.  
The thermal resistance depends on printed circuit board layout. To dissipate the heat efficiently away from Flip Chip bumps, it is better to make copper planes the largest possible as well as considering thermal vias usage.

Table 4. Recommended operating conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{ccA}$	Power supply		1.62	1.8	1.92	V
$V_{bat}$	Battery power supply		3.1		5	V
$I_{out}$	$V_{ccB}$ output current		0.10	100	200	mA
$C_{bat}$	External battery capacitance	Ceramic capacitor		2.20		$\mu F$
$C_{out}^{(1)}$	External output capacitance	$T_a = -40\text{ }^{\circ}C$ to $+85\text{ }^{\circ}C$ , $V_{bias} = 0\text{ V}$ to $3.3\text{ V}$ Multi-layer ceramic capacitor type like: C20RX7R1C225K	1.4 (-35%)	2.20	3.0 (+35%)	$\mu F$
ESR <sup>(2)</sup>	Equivalent series resistance for $C_{out}$	$F = 1\text{ Hz}$ to $10\text{ MHz}$ Multi-layer ceramic capacitor type like: C20RX7R1C225K	0	3	200	m $\Omega$
$T_{aop}$	Ambient operating temperature		-30	25	85	$^{\circ}C$
$T_{jop}$	Junction operating temperature		-30	25	125	$^{\circ}C$
$P_{dop}$	Maximum power dissipation	$P_{dop} = (T_{jop} - T_{aop})/R_{th(j-a)}$			625	mW
Enable	Enable input voltage		0		$V_{ccA}$	V
External pins (without WP and CD)	CMD-B, CLK-B, Dat0-B, Dat1-B, Dat2-B, Dat3-B		0		$V_{ccB}$	V
Internal pins (except Enable, with WP and CD)	WP, CD, Dat123.dir, CMD.dir, CMD.h, CLK.h, CLK-f, Dat0.dir, Dat0.h, Dat1.h, Dat2.h, Dat3.h		0		$V_{ccA}$	V

1.  $C_{out} = 2.2\text{ }\mu F$  is minimum allowable capacitance value to guarantee LDO stability

2. Values for ESR include the  $V_{ccB} - C_{out}$  resistance path and  $C_{out} - GND$  resistance path. These resistance paths need to be minimized in PCB design.

Table 5. LDO - Current levels in recommended operating conditions

Symbol	Parameter	Test conditions <sup>(1)</sup>	Min.	Typ.	Max.	Unit
$I_{Q\_OFF}$	Quiescent current consumption $I_{CCA\_OFF}$	$V_{EN} = 0.4\text{ V}$ , $V_{bat} = 3.4\text{ V}$ , $V_{CCA} = 1.92\text{ V}$ *.dir, *.h, *-B = GND, WP = CD = $V_{CCA}$ All other pins floating			1	$\mu\text{A}$
	Quiescent current consumption $I_{bat\_OFF}$	$V_{EN} = 0.4\text{ V}$ , $V_{bat} = 5\text{ V}$ , $V_{CCA} = 1.92\text{ V}$ *.dir, *.h, *-B = GND All other pins floating			1	$\mu\text{A}$
$I_{Q\_ON}$	Quiescent current consumption (Ground pin current) $I_{bat} + I_{CCA}$	Level shifter disactivated *.dir = 0 V, $V_{bat} = 3.4\text{ V}$				
		$I_{out} = 100\text{ }\mu\text{A}$		160	220	$\mu\text{A}$
		$I_{out} = 50\text{ mA}$		320	375	$\mu\text{A}$
		$V_{EN} = V_{CCA} = V_{CLK.h} = 1.8\text{ V}$ All other pins floating				
		$I_{out} = 100\text{ mA}$		470	550	$\mu\text{A}$
		$I_{out} = 200\text{ mA}$		750	900	$\mu\text{A}$

1. See [Note: on page 3](#) for definition of collective names of pins, for example \*.dir

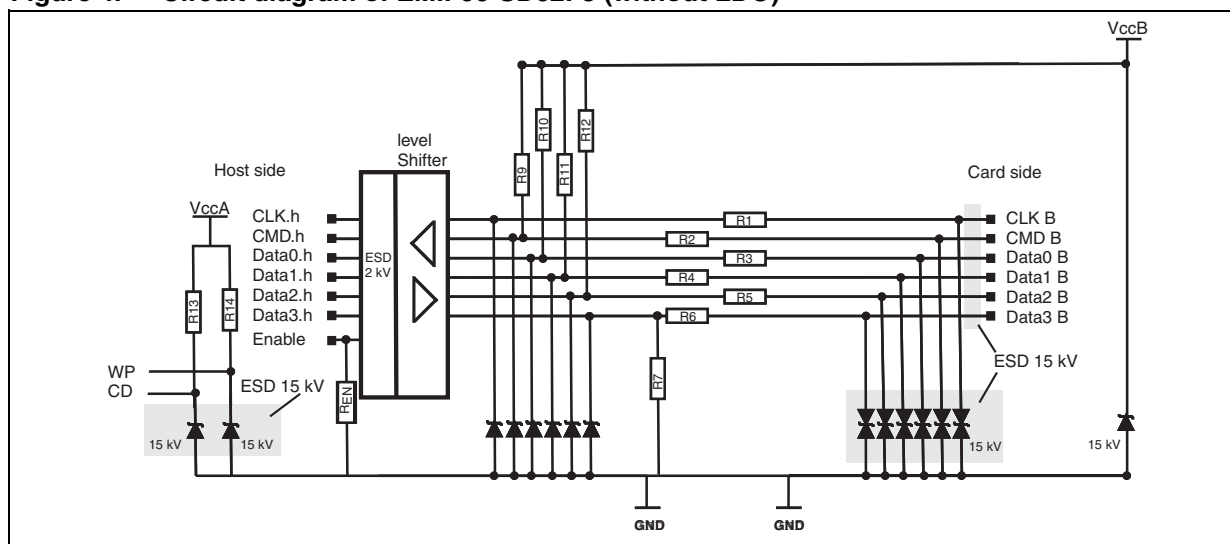
Table 6. Level shifter - Current levels in recommended operating conditions

Symbol	Parameter	Test conditions <sup>(1)</sup>	Min.	Typ.	Max.	Unit
$I_{CCA\_ON}$	Quiescent current on $V_{CCA}$	$V_{EN} = V_{CCA} = 1.92\text{ V}$ , $V_{bat} = 3.4\text{ V}$ *.dir = $V_{CCA}$ , $V_{iA} = *.h = V_{CCA}$		3	10	$\mu\text{A}$
$I_{CCB\_ON}$	Quiescent current on $V_{CCB}$	$V_{EN} = V_{CCA} = 1.92\text{ V}$ , $V_{bat} = 3.4\text{ V}$ *.dir = 0 V, $V_{CCB} = 3.05\text{ V}$ , $V_{iB} = V_{CCB}$		15	30	$\mu\text{A}$

1. See [Note: on page 3](#) for definition of collective names of pins, for example \*.dir

### 3 Passive integration and low pass filter

Figure 4. Circuit diagram of EMIF06-SD02F3 (without LDO)



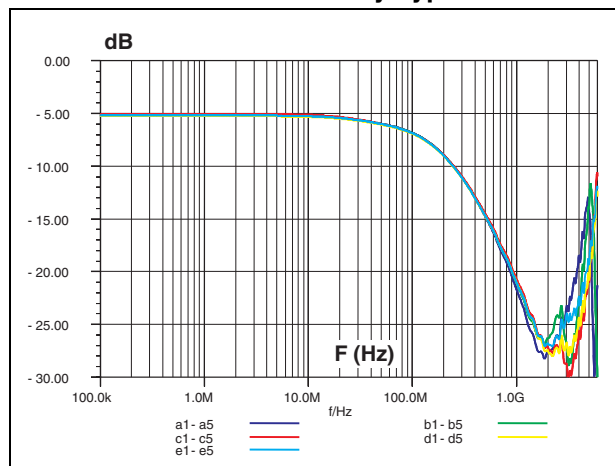
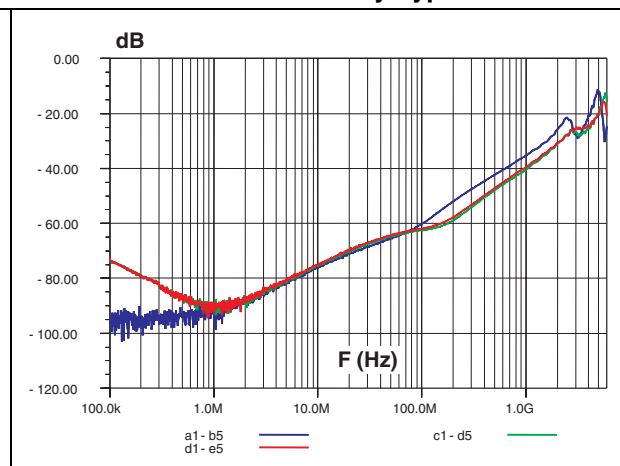
Note:  $V_{BR}$  in 14 V technology for pins: CMD-B, CLK-B, Dat0-B, Dat1-B, Dat2-B, Dat3-B, WP, CD  
 $V_{BR}$  in 8 V technology for pins: Vcc-B, CLK.h, CLK-f, CMD.h, Dat0.h, Dat1.h, Dat2.h, Dat3.h



Table 7. Components

Symbol	Parameter	Test conditions <sup>(1)</sup>	Min.	Typ.	Max.	Unit
$C_{in-A}$	Input capacitance for A side	$V_{bat} = 3.4\text{ V}$ , *.dir = $V_{EN} = V_{CCA}$ $F = 1\text{ MHz}$ , $V_{dc} = 0\text{ V}$ , $\pm 30\text{ mV}$ , $V_{AC} = 30\text{ mV}$		5	35	pF
$C_{in-B}$	Input capacitance for B side	$V_{bat} = 3.4\text{ V}$ , *.dir = GND, $V_{EN} = V_{CCA}$ $F = 1\text{ MHz}$ , $V_{dc} = 0\text{ V}$ , $\pm 30\text{ mV}$ , $V_{AC} = 30\text{ mV}$		25	35	pF
$C_{EMIF}$	Capacitance seen on B side from EMIF filter			15		pF
R1, R2, R3, R4, R5, R6 <sup>(2)</sup>	EMIF resistors <sup>(3)</sup>	$T_j = 25\text{ }^{\circ}\text{C}$		40		$\Omega$
$R_{line}$	Line resistance	at 20 mA	40	50	60	$\Omega$
R10, R11, R12	EMIF resistors <sup>(4)</sup>	$T_j = 25\text{ }^{\circ}\text{C}$	49	70	91	k $\Omega$
R9	EMIF resistor <sup>(4)</sup>	$T_j = 25\text{ }^{\circ}\text{C}$	10.5	15	19.5	k $\Omega$
R7	EMIF resistor <sup>(4)</sup>	$T_j = 25\text{ }^{\circ}\text{C}$	329	470	611	k $\Omega$
R13	EMIF resistor <sup>(4)</sup>	$T_j = 25\text{ }^{\circ}\text{C}$	70	100	130	k $\Omega$
R14	EMIF resistor <sup>(4)</sup>	$T_j = 25\text{ }^{\circ}\text{C}$	70	100	130	k $\Omega$
$R_{EN}$	Resistor <sup>(4)</sup>	$T_j = 25\text{ }^{\circ}\text{C}$		500		k $\Omega$

1. See [Note: on page 3](#) for definition of collective names of pins, for example \*.dir
2. These values are guaranteed by design and statistical process control.
3. 20% tolerance in resistance value
4. 30% tolerance in resistance value

Figure 5. Frequency response with level shifters internally bypassed<sup>(1)</sup>Figure 6. Crosstalk response with level shifters internally bypassed<sup>(1)</sup>

1. Measurement in 50  $\Omega$  environment

## 4 Data transmission

All values in the tables below are guaranteed across the operating temperature and voltage range unless otherwise specified.

**Table 8. DC voltage levels on host side**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IHA}$	High level input voltage		$0.65 \times V_{CCA}$	$V_{CCA}$		V
$V_{ILA}$	Low level input voltage		0	0	$0.35 \times V_{CCA}$	V
$V_{OHA}$	High level output voltage	$I_{oh} = -6 \text{ mA}$	$V_{CCA} - 0.45$			V
$V_{OLA}$	Low level output voltage	$I_{ol} = 7 \text{ mA}$		0	0.45	V

**Table 9. DC voltage levels on SD side**

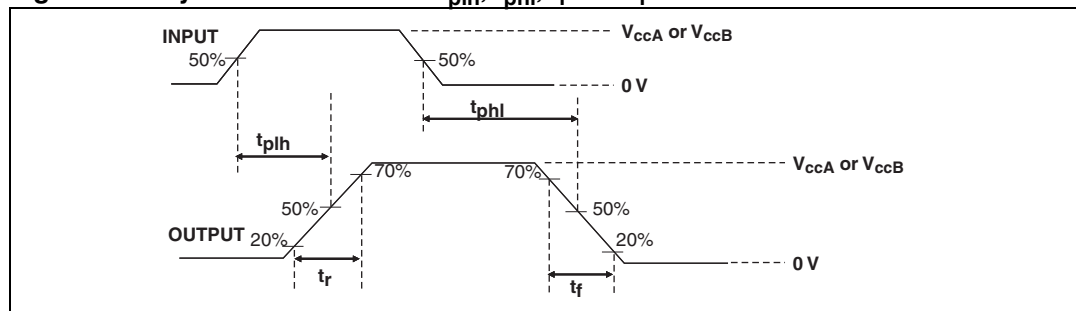
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IHB}$	High level input voltage		$0.7 \times V_{CCB}^{(1)}$	$V_{CCB}$		V
$V_{ILB}$	Low level input voltage			0	$0.3 \times V_{CCB}^{(1)}$	V
$V_{OHB}$	High level output voltage	$I_{oh} = -8 \text{ mA}$	$V_{CCB}^{(1)} - 0.7$	2.9		V
$V_{OLB}$	Low voltage output voltage	$I_{ol} = 8 \text{ mA}$		0	0.7	V

1.  $V_{CCB}$  is defined in power supply block.

**Table 10. DC current levels**

Symbol	Parameter	Test conditions <sup>(1)</sup>	Min.	Typ.	Max.	Unit
$I_{LH}$	Leakage current on host pin	$V_{EN} = *.dir = V_{CCA} = 1.92 \text{ V}$ , $V_{iA} = V_{CCA}$ or GND, $V_{bat} = 3.4 \text{ V}$			5	$\mu\text{A}$
$I_{LSD}$	Leakage current on SD pin	$V_{bat} = 3.4 \text{ V}$ , $V_{CLK.h} = V_{CCA}$ , $V_{CMD} = V_{Dat0} = V_{Dat1} = V_{Dat2} = V_{CCB}$ $V_{Dat3} = *.dir = \text{GND}$			5	$\mu\text{A}$
$I_{SCH}$	Short circuit current on host side	SD input = H, host = 0 V SD input = 0 V, host = $V_{CCA} = 1.8 \text{ V}$ $*.dir = 0 \text{ V}$ , $V_{bat} = 3.4 \text{ V}$ , $T_j = 25 \text{ }^\circ\text{C}$		25		mA
$I_{SCSD}$	Short circuit current on SD side	Host input = H, SD = 0 V Host input = L, SD = $V_{CCB}$ , $T_j = 25 \text{ }^\circ\text{C}$ $*.dir = V_{CCA} = 1.8 \text{ V}$ , $V_{bat} = 3.4 \text{ V}$		60		mA

1. See [Note: on page 3](#) for definition of collective names of pins, for example \*.dir

**Figure 7. Symbol definitions of  $t_{plh}$ ,  $t_{phl}$ ,  $t_r$  and  $t_f$  for AC characteristics in Table 11****Table 11. AC characteristics**

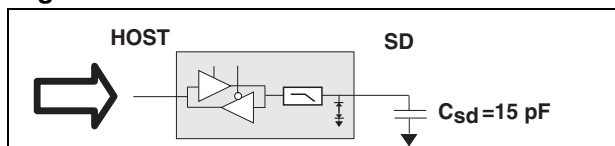
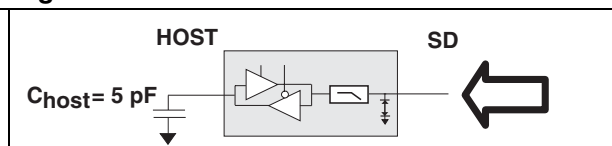
Symbol	Parameter	Test conditions		Min	Typ	Max	Unit
t <sub>phl</sub>	Propagation delay hl from host to SD	Section 4.1			3.5	7	ns
t <sub>plh</sub>	Propagation delay lh from host to SD				3.5	7	
t <sub>phl</sub>	Propagation delay hl from SD to host	Section 4.2			3	7	ns
t <sub>plh</sub>	Propagation delay lh from SD to host				3	7	
t <sub>r</sub>	Rise time from host to SD	Section 4.1			1.5	3	ns
	Rise time from SD to host	Section 4.2			0.5	3	
t <sub>f</sub>	Fall time from host to SD	Section 4.1			1.9	3	ns
	Fall time from SD to host	Section 4.2			0.5	3	
t <sub>skew</sub>	Delay differences from host to SD	Section 4.1	Section 4.3	-1.5	0	1.5	ns
t <sub>skew.f</sub>	t <sub>skew</sub> delay from SD to host	Section 4.2	Section 4.4	-1.5	0	1.5	ns
t <sub>p_clkf</sub>	Propagation delay for CLK feedback				6.5	14	ns
t <sub>r_clkf</sub>	Rise time for CLK feedback	Section 4.2			0.5	3	ns
t <sub>f_clkf</sub>	Fall time for CLK feedback	Section 4.2			0.5	3	ns

## 4.1 Test circuit from host to SD

Test circuit from host to SD is shown in Figure 8. Timings are measured for the whole line cell (shifter + EMI + ESD) on an external load  $C_{sd} = 15$  pF (board capacitance 5 pF + SD card capacitance 10 pF).

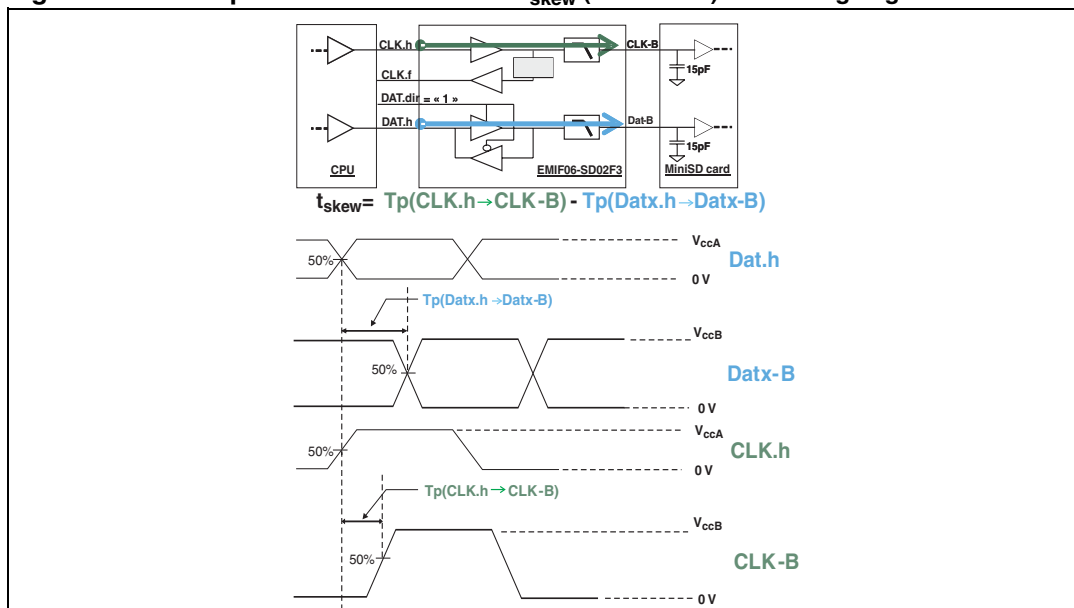
## 4.2 Test circuit from SD to host

Test circuit from SD to host is shown in Figure 9. Timings are measured for the whole line cell (shifter + EMI + ESD) on an external load  $C_{host} = 5$  pF (board capacitance + host capacitance).

**Figure 8. Test circuit from host to SD****Figure 9. Test circuit from SD to host**

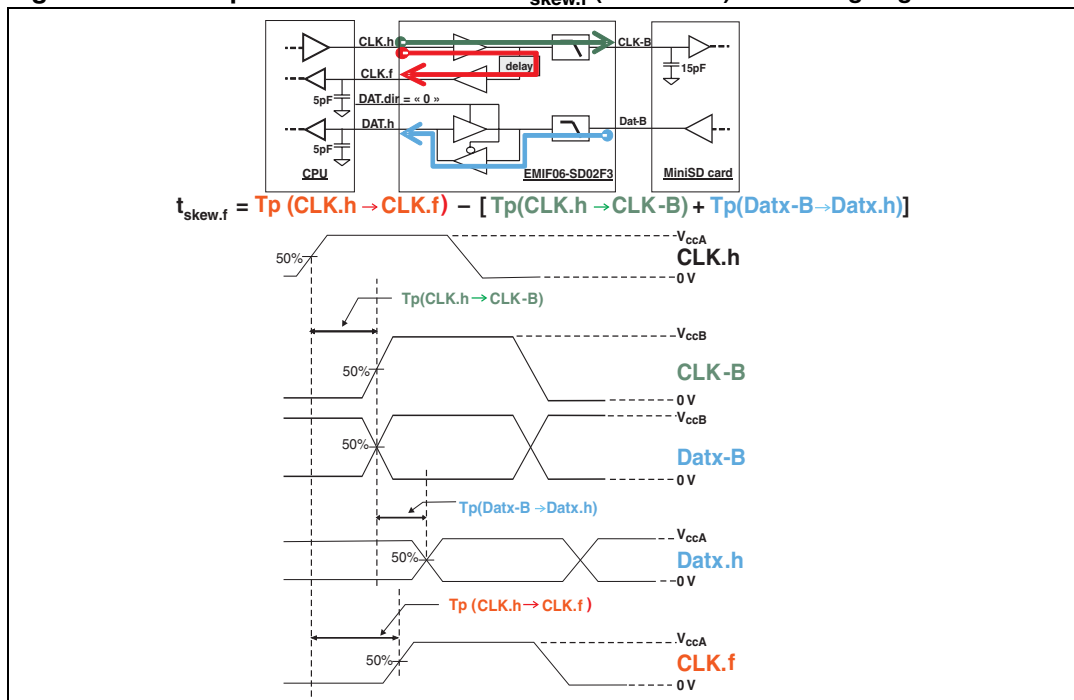
### 4.3 Measurement of $t_{\text{skew}}$ (SD to host) from rising edge CLK.h

Figure 10. Example of measurement of  $t_{\text{skew}}$  (SD to host) from rising edge CLK.h



### 4.4 Measurement of $t_{\text{skew.f}}$ (read mode) from rising edge CLK.h

Figure 11. Example of measurement of  $t_{\text{skew.f}}$  (read mode) from rising edge CLK.h

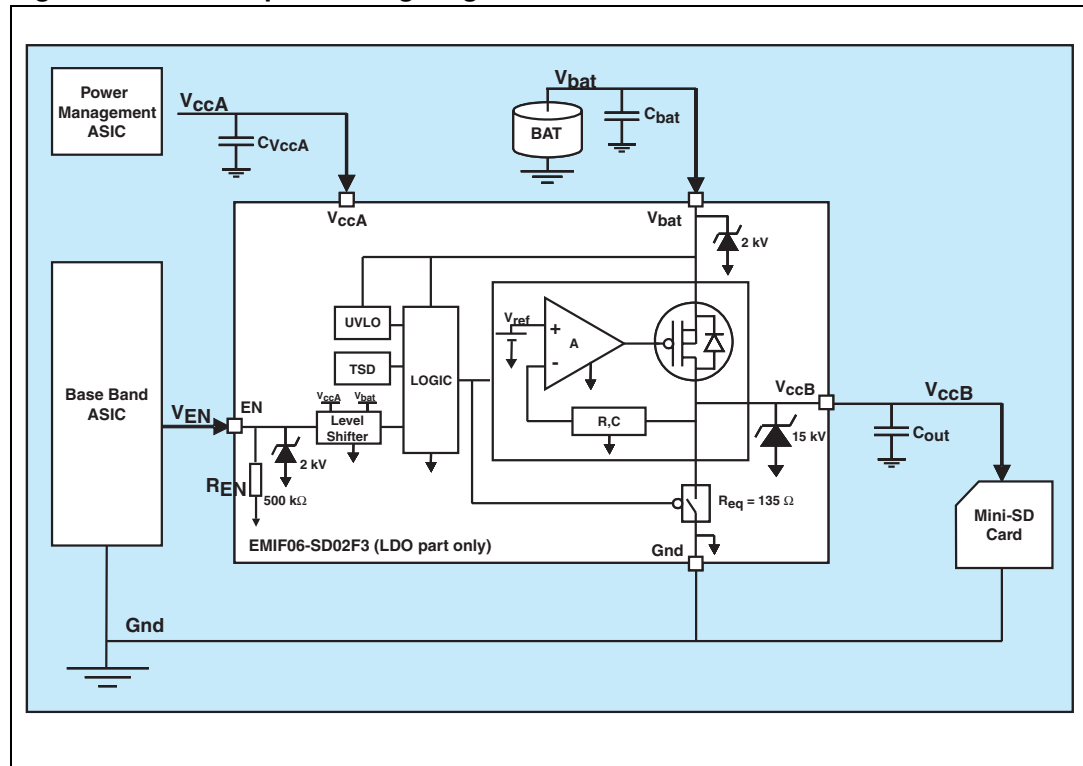


Datx.h = Dat0.h, Dat1.h, Dat2.h, Dat3.h, CMD.h

Datx-B = Dat0-B, Dat1-B, Dat2-B, Dat3-B, CMD.B

## 5 Low drop out voltage regulator

Figure 12. Low drop out voltage regulator schematic



**Table 12. Static parameters,  $V_{EN} = V_{CCA}$  unless otherwise specified, level shifter disactivated, \*.dir = 0, CLK.h =  $V_{CCA}$ , all other pins floating**

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
$V_{out}$	Regulated output voltage ( $V_{CCB}$ )	$V_{bat} = 3.4\text{ V}$ $I_{out} = 100\text{ mA}$ $T_j = 25\text{ °C}$		2.81 (-3%)	2.90	2.99 (+3%)	V
		$V_{bat} = 3.4\text{ V}$ $I_{out} = 100\text{ mA}$ $T_j = -30\text{ to }125\text{ °C}$		2.81 (-3%)		2.99 (+3%)	V
		$V_{bat} = 3.1\text{ to }5\text{ V}$ $I_{out} = 0.1\text{ to }200\text{ mA}$ $T_j = -30\text{ to }125\text{ °C}$		2.75 (-5%)		3.05 (+5%)	V
LiR	Line regulation	$V_{bat} = 3.4\text{ to }5\text{ V}$ ( <a href="#">Section 5.1</a> ) $I_{out} = 100\text{ mA}$ $T_j = 25\text{ °C}$			3	20	mV
LdR	Load regulation	$V_{bat} = 3.4\text{ V}$ $I_{out} = 1\text{ to }200\text{ mA}$ ( <a href="#">Section 5.2</a> ) $T_j = 25\text{ °C}$			50	100	mV
$V_{DO}$	Dropout voltage	$V_{out(nom)} - 100\text{ mV}$ ( <a href="#">Section 5.3</a> ) $T_j = -30\text{ to }85\text{ °C}$	$I_{out} = 50\text{ mA}$		25	37	mV
			$I_{out} = 100\text{ mA}$		50	75	mV
			$I_{out} = 200\text{ mA}$		100	150	mV
$I_{SC}$	Short circuit current limitation	$V_{bat} = 5\text{ V}$ $V_{out} = 0\text{ V}$ $T_j = 25\text{ °C}$			500		mA
TSD	Thermal shutdown temperature	$V_{bat} = 3.4\text{ V}$	Shutdown (Temp ↑)		150		°C
			Reset (Temp ↓)		130		°C
			Hysteresis		20		°C
UVLO	Under voltage lockout	$T_j = -30\text{ to }125\text{ °C}$	Shutdown ( $V_{bat} \downarrow$ )	2.3	2.5	2.7	V
			Reset ( $V_{bat} \uparrow$ )	2.35	2.55	2.75	V
			Hysteresis		50		mV

Table 13. Dynamic parameters ( $V_{EN} = V_{CCA}$  unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
LiTr	Line transient peak voltage	$V_{bat} = 3.4 \text{ V} \uparrow \downarrow 4 \text{ V}$ , $t_{tr} = 30 \mu\text{s}$ , $I_{out} = 200 \text{ mA}$ $T_j = 25^\circ\text{C}$ (Section 5.1) $C_{out} = 2.2 \mu\text{F}$ , $\text{ESR} = 5 \text{ m}\Omega$		4.2		mV
LdTr	Load transient peak voltage	$I_{out} = 1 \text{ mA} \uparrow \downarrow 200 \text{ mA}$ , $t_{tr} = 10 \mu\text{s}$ , $V_{bat} = 3.4 \text{ V}$ $T_j = 25^\circ\text{C}$ (Section 5.2) $C_{out} = 2.2 \mu\text{F}$ , $\text{ESR} = 5 \text{ m}\Omega$		9		mV
PSRR	Power supply rejection ratio	$V_{bat} = 3.4 \text{ V}$ $I_{out} = 100 \text{ mA}$ $T_j = 25^\circ\text{C}$ $C_{out} = 2.2 \mu\text{F}$ , $\text{ESR} = 5 \text{ m}\Omega$	$F = 1 \text{ kHz}$		45	db
			$F = 10 \text{ kHz}$		35	db
$T_{start}$	Settling time	$V_{out} \uparrow 95\% \text{ Nom}$ , $V_{bat} = 5 \text{ V}$ , $I_{out} = 200 \text{ mA}$ $T_j = -30^\circ\text{C}$ to $125^\circ\text{C}$ $C_{out} = 2.2 \mu\text{F}$ , Enable L $\rightarrow$ H		30	200	$\mu\text{s}$
$T_{stop}$	Discharge time	$V_{out} \downarrow 10\% \text{ Nom}$ , $V_{bat} = 3.4 \text{ V}$ , $I_{out} = 1 \text{ mA}$ $T_j = 25^\circ\text{C}$ $C_{out} = 2.2 \mu\text{F}$ , Enable H $\rightarrow$ L		600		$\mu\text{s}$

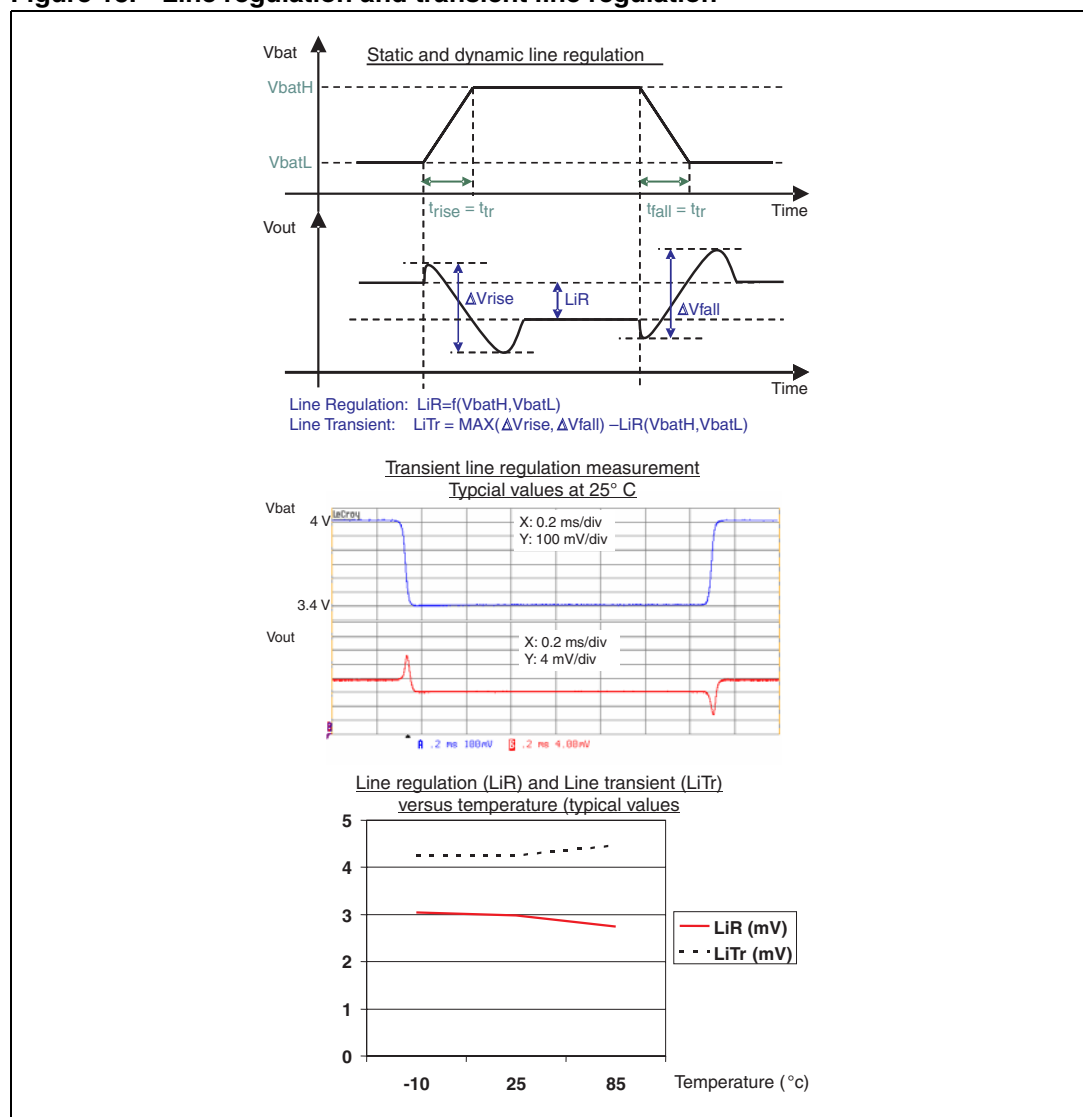
## 5.1 Line regulation and transient line regulation

The line regulation (LiR) is a static variable that indicates the change in the output voltage of the voltage controller  $\Delta V_{out}$  (at constant load) when there is a change  $\Delta V_{bat}$  at the input voltage. By contrast the line transient response (LiTr) represents dynamic peak value to be observed during the change in input voltage.

Thermal effects due to changes in the junction temperature are circumvented with pulsed voltage during the test and are to be taken into account separately.

Figure 13 shows the boundary conditions for  $t_{rise}$ ,  $t_{fall}$ , and  $\Delta V_{bat}$  to be taken as the basis of the measurement of the line transient response without additional decoupling of the supply voltage by a buffer capacity  $C_{bat}$ . The values defined in the specification apply, however, only in the case of decoupling of the supply voltage with such a capacity  $C_{bat}$ , as a result of which the values for  $t_{rise}$  and  $t_{fall}$  are influenced to some extent.

**Figure 13. Line regulation and transient line regulation**





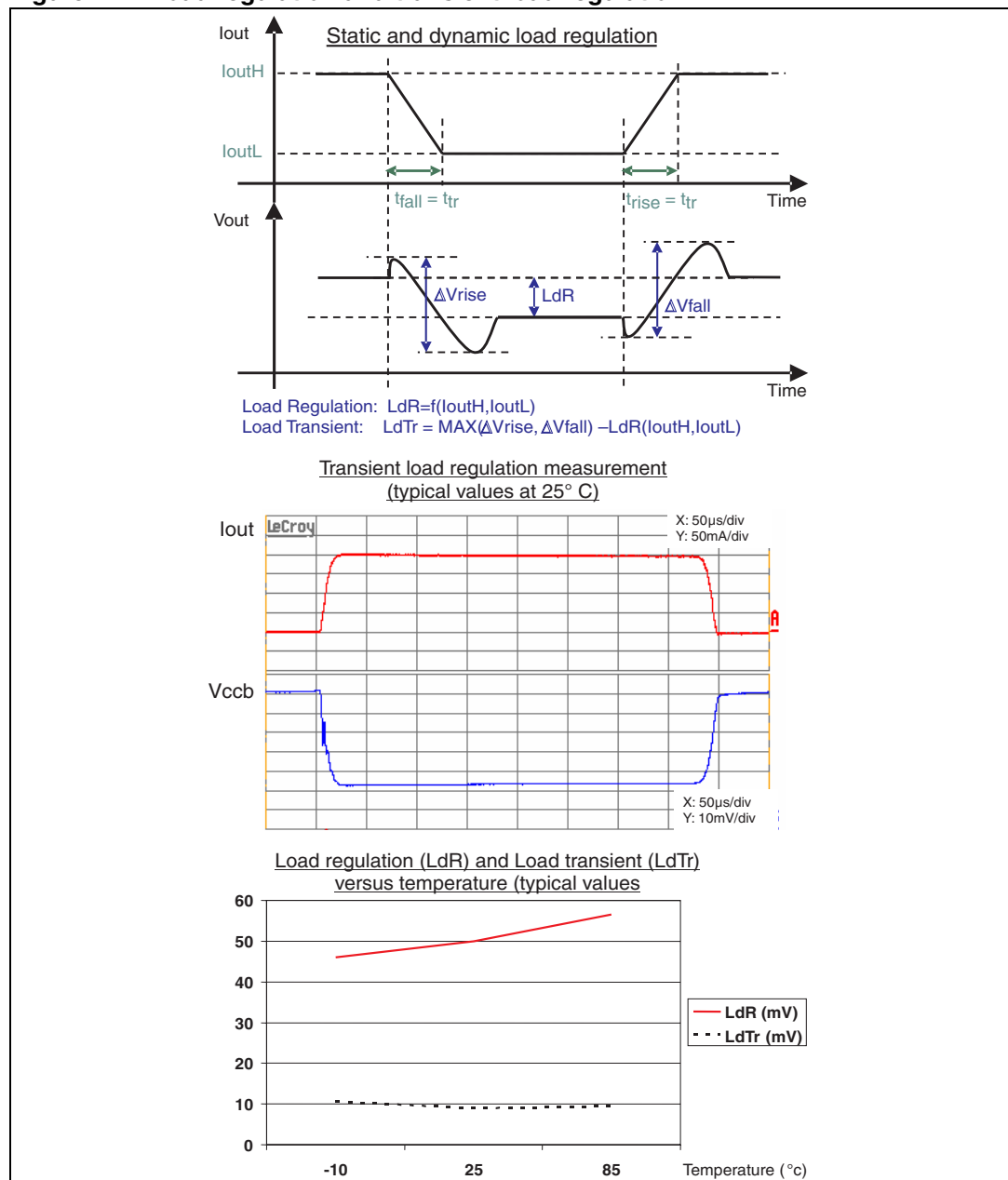
## 5.2 Load regulation and transient load regulation

The load regulation (LdR) is a static variable that indicates the change in output voltage of the voltage controller  $\Delta V_{out}$  (at constant input voltage) in the event of a change in the load current  $\Delta I_{out}$ . By contrast the load transient response (LdTr) represents the dynamic peak value to be observed during load variation.

Thermal effects due to changes in the junction temperature are circumvented by testing with pulsed load and are to be taken into account separately.

The figure shows the boundary conditions for  $t_{rise}$ ,  $t_{fall}$ , and  $\Delta I_{out}$  to be taken as the basis for the measurement of the load transient response.

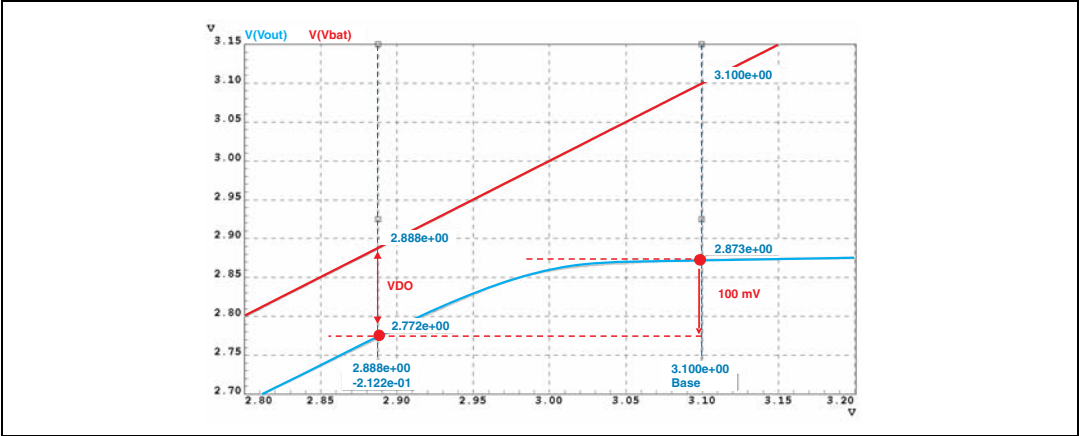
**Figure 14. Load regulation and transient load regulation**



5.3 Dropout definition

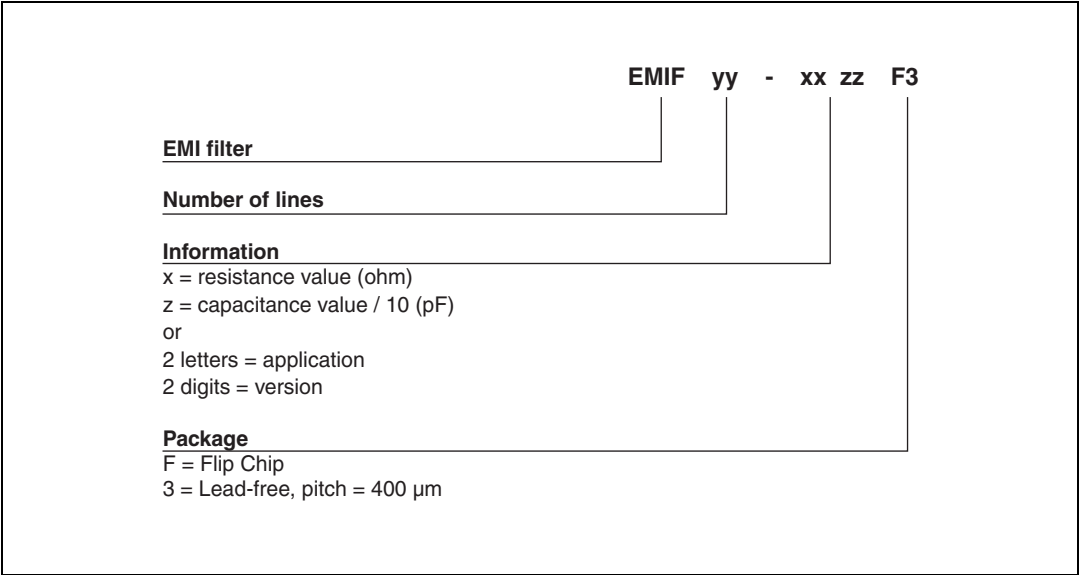
The dropout voltage ( $V_{DO}$ ) is measured by decreasing the input voltage till the output voltage will drop by 100 mV compared to the output voltage measured at the specified minimum supply voltage (3.1 V). Worst case for dropout is maximum die temperature and maximum current load. This is done statically.

Figure 15. Dropout definition



6 Ordering information scheme

Figure 16. Ordering information scheme



# 7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

Figure 17. Flip Chip dimensions

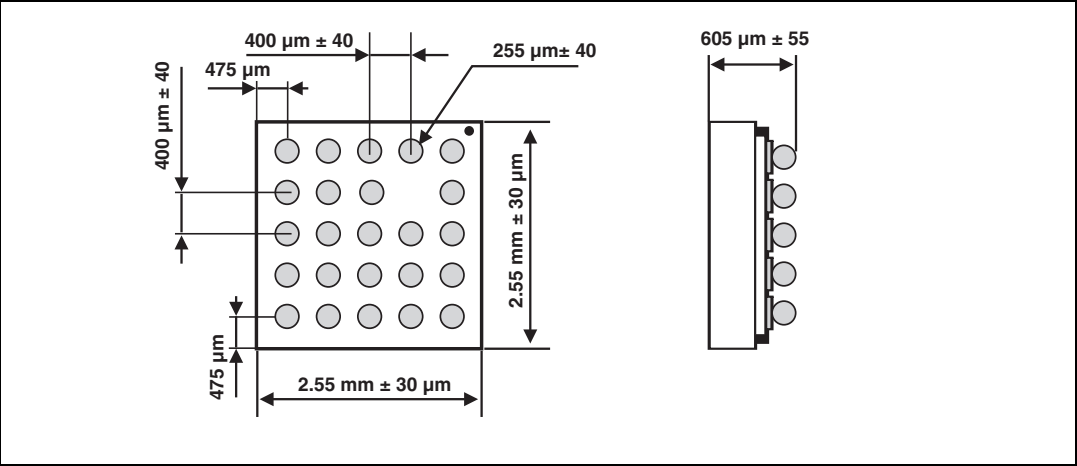


Figure 18. Footprint recommendations

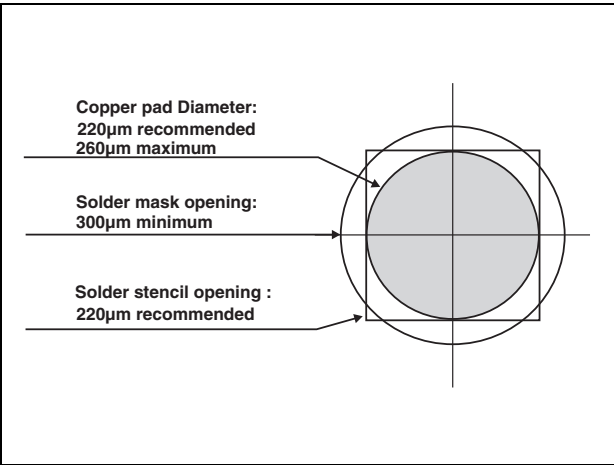


Figure 19. Marking

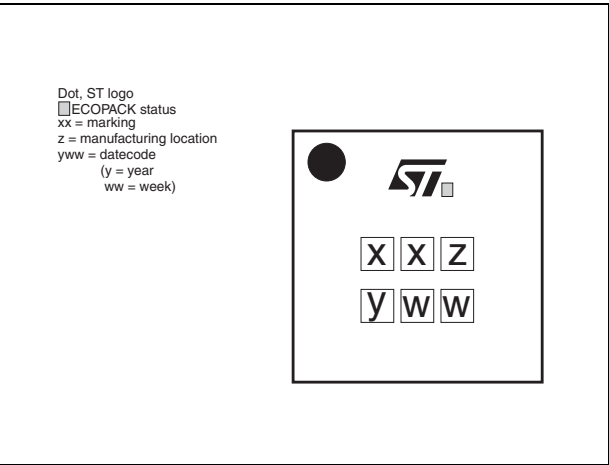
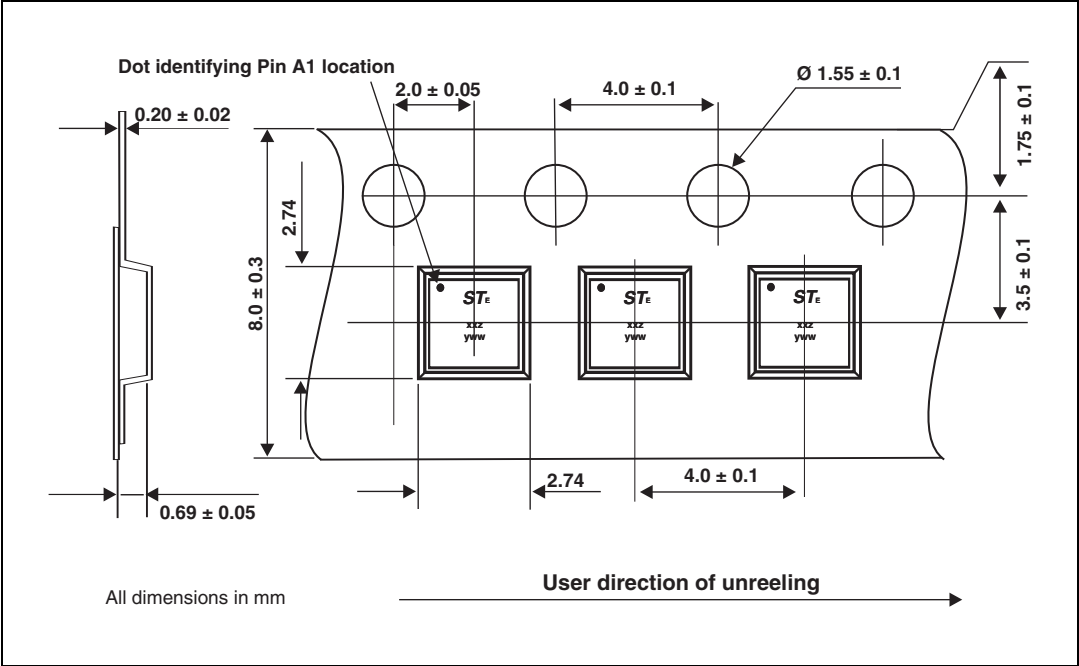


Figure 20. Flip Chip tape and reel specifications



## 8 Ordering information

Table 14. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
EMIF06-SD02F3	HF	Flip Chip	7.45 mg	5000	Tape and reel (7")

Note: More information is available in the application note :  
 AN2348 : "Flip Chip : Package description and recommendations for use"  
 AN1751 : EMI Filters: Recommendations and measurements

## 9 Revision history

Table 15. Document revision history

Date	Revision	Changes
05-Feb-2007	1	First issue
26-Feb-2007	2	Last corrections.
19-Sep-2007	3	Updated graphic in <a href="#">Section 5.1</a> .
10-Feb-2010	4	Updated pocket depth in <a href="#">Figure 20</a> .

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